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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GERARD CHAUVEL, SERGE LASSERRE, and
DOMINIQUE D'INVERNO

Appeal 2009-005169
Application 10/631,308
Technology Center 2100

Decided: June 11, 2010

Before ST. JOHN COURTENAY III, CAROLYN D. THOMAS, and DEBRA K. STEPHENS, *Administrative Patent Judges*.

COURTENAY, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants seek our review under 35 U.S.C. § 134 of the Examiner's final decision rejecting claims 1-16, 18-27, and 30-41. Claims 17, 28, and

29 are cancelled. We have jurisdiction over the appeal under 35 U.S.C. § 6(b).

We Reverse.

Claims 1 and 8 are illustrative:

1. A processor, comprising:
a core;
a multi-entry stack contained in said core and usable in at least a stack-based instruction set and comprising a plurality of entries, all of said entries of said multi-entry stack correspond to a subset of entries at the top of a main stack implemented in memory outside said core;

logic contained in said core and coupled to said stack, the logic manages the stack; and

a plurality of registers contained in said core and coupled to the logic and addressable through a second instruction set that provides register-based and memory-based operations;

wherein said logic executes instructions from both said stack-based instruction set and said second instruction set; and

an instruction fetch logic contained in said core, said instruction fetch logic receives at least stack-based instructions from the stack-based instruction set.

8. A method of processing instructions in a processor, comprising:

fetch logic in a core of the processor receiving instructions from a first instruction set which comprises stack-based instructions;

> said fetch logic receiving instructions from a second instruction set which comprises memory-based and register-based instructions; and
>
> executing said received instructions from the first and second instruction sets in said core.

Appellants appeal the following rejections:

1. Claims 8-11 under 35 U.S.C. § 102(b) as anticipated by Feierbach (US 6,088,786, Jul. 11, 2000)

2. Claims 1, 2, 4, 6, and 7 under 35 U.S.C. § 103(a) as unpatentable over Feierbach and Batten (US 6,256,725 Jul. 3, 2001).

3. Claim 3 under 35 U.S.C. § 103(a) as unpatentable over Feierbach Batten and Patel (US 6,826,749, Nov. 30, 2004).

4. Claim 5 under 35 U.S.C. § 103(a) as unpatentable over Feierbach, Batten and Gee (US 6,374,286, Apr. 16, 2002).

5. Claims 12-15, 18-24, and 27 under 35 U.S.C. § 103(a) as unpatentable over Feierbach, Batten, Patel, and Hennessy ("Computer Architecture: A Quantitive Approach.")

6. Claims 16 and 26 under 35 § 103(a) as unpatentable over Feierbach, Patel, Batten, Hennessy, and Gee.

7. Claim 25 under 35 U.S.C. § 103(a) as unpatentable over Feierbach, Batten, Patel, Hennessy, Hendler (US 6,473,777, Oct. 29, 2002), and Brassac (US 6,928,539 Aug. 9, 2005)

8. Claims 30-35, 37, and 41 under 35 U.S.C. § 103(a) as unpatentable over Feierbach and Hendler.

9. Claim 36 under 35 U.S.C. § 103(a) as unpatentable over Feierbach, Hendler and Patel.

10. Claims 38-40 under 35 U.S.C. §103(a) as unpatentable over Feierbach, Hendler, and Gee.

ISSUE

Did the Examiner err in finding that Feierbach discloses (§ 102) or suggests (§ 103) a core of a processor that executes a first and second set of instructions, wherein the second set of instructions comprises memory-based and register based instructions?

FACTUAL FINDINGS

1. The Examiner admits that Feierbach failed to teach logic that executes instructions from both said stack-based instruction set and said second instruction set. (Ans. 7). The Examiner relied on Batten as teaching this limitation. (Id.).

2. Feierbach discloses a microprocessor that includes logic that distributes processing of instructions between the stack based processor and the register based processor. *The logic is coupled to receive a plurality of stack based instructions*. (Col. 3, ll. 12-15).

3. The logic is configured to determine which of the plurality of stack based instructions are *regular stack instructions,* and which are *extended stack instructions*. (Col. 3, ll. 15-23).

ANALYSIS

The Appellants argue that Feierbach does not disclose "a multi-entry stack contained in said core and usable in at least a stack-based instruction

set and . . . a plurality of registers contained in said core and coupled to the logic and addressable through a second instruction set." (App. Br. 12).

We agree.

More specifically, as discussed *infra*, we find that Feierbach fails to disclose or suggest a core of a processor that is capable of processing two instructions sets, as required by the commensurate language of each independent claim before us on appeal.

The Examiner admits in rejecting claims 1 and 12 under §103 that Feierbach fails to disclose logic that executes instructions from both said stack-based instruction set and said second instruction set. (FF 1). We note that this limitation ("executing said received instructions from the first and second instructions sets in said core") is recited in commensurate form in independent claim 8 which stands rejected under § 102 over Feierbach and Official Notice. (*See* the Examiner's taking of Official Notice, Ans. 4). We find the Examiner's reliance upon Official Notice (Ans. 4) is misplaced in rejecting claim 8 under § 102.

As noted above, we find Feierbach discloses microprocessor logic that directs instructions between a *stack-based processor* and *a register-based processor.* (FF 2-3). Therefore, we find Feierbach does not disclose or suggest *a core* within a processor that processes *two distinct instructions sets* as required by the commensurate claim language of independent claims 1, 8, 12, and 30.

Based on the record before us, we find the Examiner erred in rejecting independent claims 1, 8, 12, and 30. Accordingly, we reverse the Examiner's rejections of claims 1, 8, 12, and 30 as well as associated dependent claims 2-7, 9-11, 13-16, 18-27, and 31-41.[1]

DECISION

We reverse the Examiner's rejections of claims 1-16, 18-27, and 30-41.

ORDER

REVERSED

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[1] Claims 1-7 and 12-41 are rejected under § 103. We do not find, nor has the Examiner established, that the secondary references cited by the Examiner cure the deficiencies of Feierbach.